

Homework 03 Solution

ECE 587, Spring 2026

Consider the following sequential program that should be implemented as a hardware component.

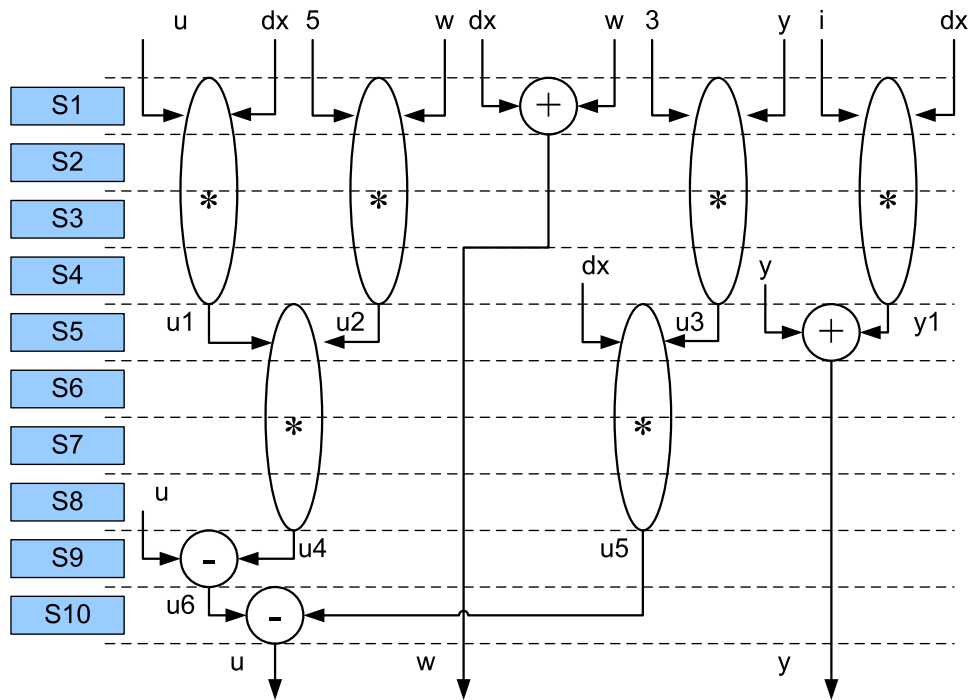
inputs/outputs: u, w, y, dx, i
temporary variables: $u1, u2, u3, u4, u5, u6, y1$

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u1 = u*dx;
u2 = 5*w;
u3 = 3*y;
y1 = i*dx;
w = w+dx;
u4 = u1*u2;
u5 = dx*u3;
y = y+y1;
u6 = u-u4;
u = u6-u5;
```

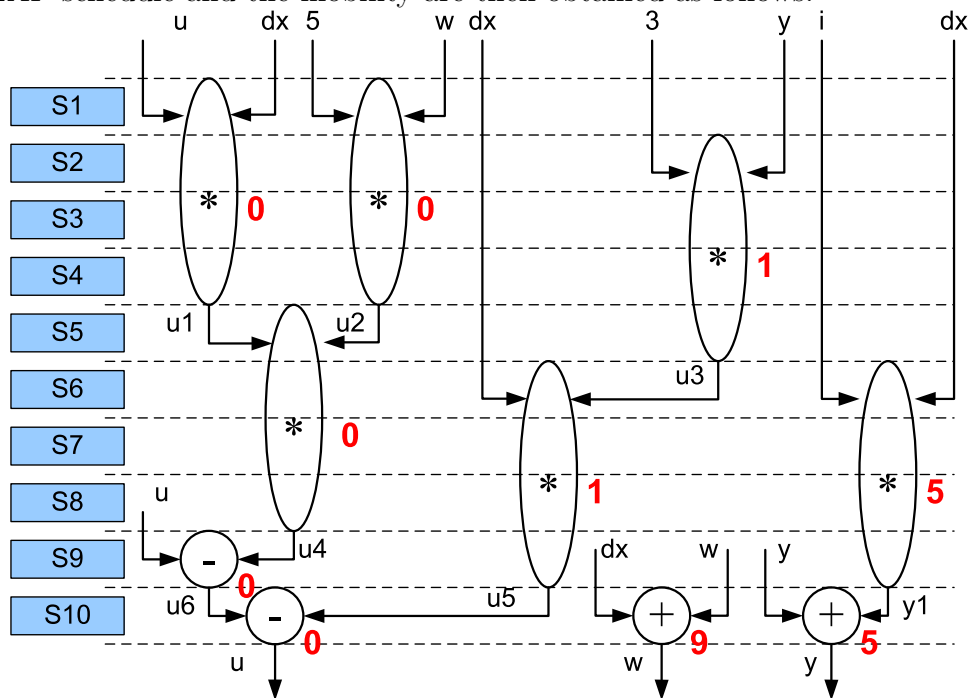
1. (2 points) Assume each multiplication takes 4 clock cycles and each addition or subtraction takes 1 clock cycle. Compute the ASAP schedule to determine the minimum execution time. Compute the ALAP schedule based on the minimum execution time.
2. (2 points) Assume there are one 2-input multiplier, which is pipelined into 4 stages, and one 2-input adder/subtractor, which is not pipelined. Perform a resource-constrained scheduling using the mobility computed from the results of 1.
3. (1 point) Determine variable lifetimes and bind variables to as few registers as possible. (Note: you don't need to consider connection cost.)

Answer:

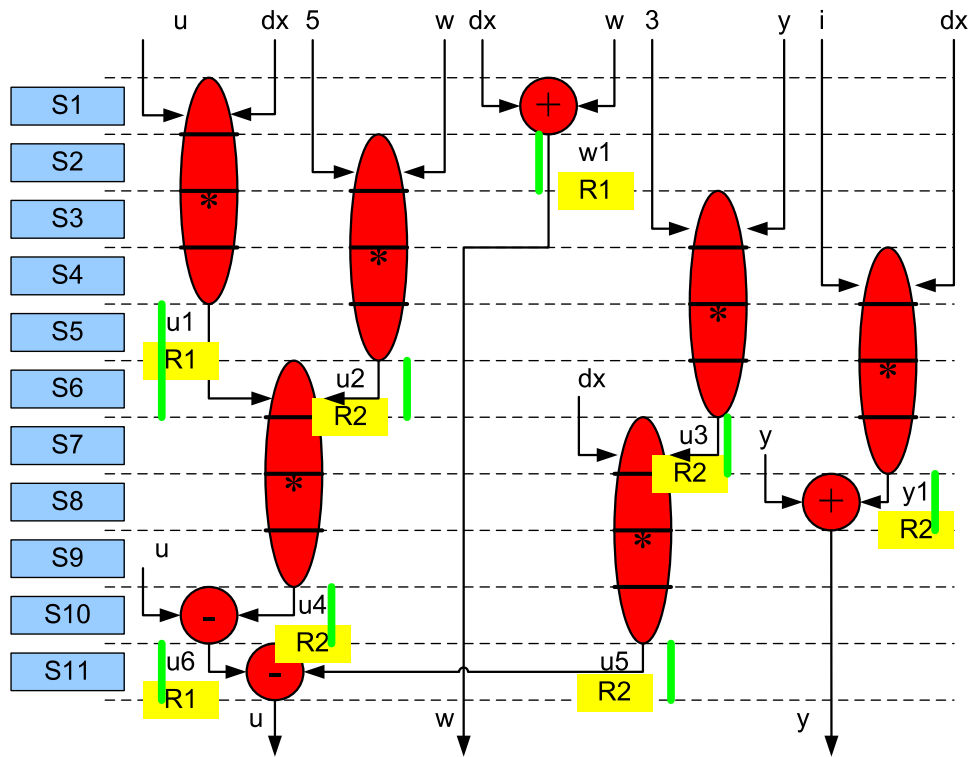
The ASAP schedule is shown in the following figure, where the minimum execution time is 10 cycles.



The ALAP schedule and the mobility are then obtained as follows.



The RC scheduling is then obtained and the variable lifetimes should be computed before 2 registers are assigned.



Note that an additional variable $w1$ is introduced to resolve a write-after-read dependency.